REMARKS

Claims 24, 36, 37, 40 and 41 are amended. Claims 1-23, 32-35, 38, and 42-44 are cancelled. Claims 45-53 are added. Claims 24-31, 36, 37, 39-41 and 45-53 are in the application for consideration.

Independent claim 24 stands rejected as being anticipated by U.S. Patent No. 6,235,581 to Chen. Claim 24 recites that the trench isolation regions comprise isolation trenches having insulating dielectric material received therein. Claim 24 also recites the forming of a conductive line over the discrete transistor source areas and over the insulating dielectric material received within the isolation trenches. Support for the same is inherent from Applicant's application as filed, for example at Fig. 6. Specifically, in such depicted preferred embodiment, conductive line materials 38/39 are received over discrete source areas 30b and over insulating dielectric material 20 received within trenches 16. Chen neither discloses nor suggests such a construction. Specifically, its alleged conductive line 17 is nowhere shown nor suggested to be received over insulating dielectric material received within its depicted trenches. Accordingly, amended independent claim 24 is neither anticipated nor rendered obvious by the '581 Chen reference. Accordingly, allowance of independent claim 24 is warranted and urged.

Claims 26 and 28 stand rejected as being obvious over the '581 Chen reference. Such claims should be allowed at least for the reasons argued

Received from < 5098383424 > at 2/4/02 6:04:07 PM [Eastern Standard Time]

above with respect to the allowability of claim 24. Allowance of such claims is urged and requested.

Independent claim 36 stands rejected as being anticipated by U.S. Patent No. 5,854,108 to Hsu et al. Independent claim 36 has been amended to include the subject matter of claim 41. Further, independent claim 36 has been amended to recite that the line of floating gates has an insulative cap having an outermost surface. Support for the same is inherent from Applicant's application as filed, for example at Figs. 7-9 and in the specification as filed at p.9, lns.13-16. The specification at page 13-14 is amended to include this inherently disclosed subject matter. Accordingly, no new matter is added thereby. Claim 36 is also amended to recite that the insulative sidewall spacer has an outermost surface which is substantially elevationally coincident with the insulative cap outermost surface. Support for the same is also inherent from Applicant's application as filed, for example at Fig.7 where each of the depicted anisotropically etched insulative sidewall spacers are shown as having an outermost surface which is substantially elevationally coincident with an adjacent insulative cap outermost surface. Hsu et al. neither discloses nor suggests the amended independent claim 36 combination.

Specifically, Hsu et al. does not form an insulative sidewall spacer in one anisotropic etching step on only the drain side and not on the source side. Fig. 5C of Hsu et al. clearly discloses its left illustrated spacer as

Received from < 5098383424 > at 2/4/02 6:04:07 PM [Eastern Standard Time]

being formed on th source side, not on the drain side as Applicant recites in claim 36. Further, material 152 of Hsu et al. is disclosed as being the control gate, and no insulative cap is shown disposed thereover. Regardless, the left illustrated anisotropically etched spacer 158 has an outermost surface which is elevationally coincident with an outermost surface of the control gate 152, and therefore not substantially elevationally coincident with an insulative cap outermost surface. Hsu et al. does not disclose Applicant's amended claim 36 insulative cap, and accordingly it is inconceivable that the reference could suggest, either expressly or impliedly, positioning an outermost surface of a component relative to another component which the reference does not even have. Accordingly, for at least these reasons, Applicant's amended independent claim 36 should be allowed, and action to that end is requested.

Independent claim 37 also stands rejected as being anticipated by Hsu et al. Such claim has been amended to recite forming a first insulative sidewall spacer in one anisotropic etching step and forming a second insulative sidewall spacer on an opposing side in another anisotropic etching step. The first and second insulative sidewall spacers are recited to have respective outermost surfaces which are substantially elevationally coincident with the insulative cap outermost surface. Again, Hsu et al. does not disclose an insulative cap, and therefore not an insulative cap outermost surface. It is virtually inconceivable that the reference could either disclose

Received from < 5098383424 > at 2/4/02 6:04:07 PM [Eastern Standard Time]

or suggest positioning an outermost surface of insulative sidewall spacers relative to a surface and structure which it does not even have in the first place. Further, the right illustrated alleged "spacer" referred to by Hsu et al. is not seen to be the equivalent of Applicant's first or second stated spacer in independent claim 37. For at least these reasons, Applicant's independent claim 37 should be allowed and action to that end is requested.

Applicant's previously remaining and amended dependent claims should be allowed as depending from allowable base claims, and for their own recited features which are neither shown nor suggested in the cited art. Further, dependent claim 39 depends from the allowable and inherently generic thereto independent claim 36, and accordingly such should now be examined and allowed in this application. Action to that end is requested.

Dependent claims 45-53 are added. Support for the same is inherent from Applicant's application as filed, for example at Fig. 6. Specifically, and by way of example only, such shows isolation trenches 16 filed with insulating dielectric material 20. Further, the depicted conductive line 40 has a substantially planar outermost surface as the top surface of material 39, and a substantially planar innermost surface as the base of material 38. Accordingly, the claims are supported from Applicant's application as filed. Neither the applied Chen or Hsu et al. references discloses the facets of Applicant's added dependent claims. Such claims should be allowed as depending from allowable base claims, and for their own recited features

Received from < 5098383424 > at 2/4/02 6:04:07 PM [Eastern Standard Time]

which are neither shown nor suggested in the cited art. Action to that end is requested.

This application is believed to be in immediate condition for allowance, and action to that end is requested.

Respectfully submitted,

Dated: 2-2-02

By: _____
Mark S. Matkin
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/768,878
Filing Date . . . . . January 23, 2001
Inventor . . . . . Graham Wolstenholme
Assignee . . . . . Micron Technology, Inc.
Group Art Unit 2812
Examiner . . . . . Richard A. Booth
Attorney's Docket No. MI55-003
Title: Methods of Forming a Line of FLASH Memory Cells

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO DECEMBER 21, 2001 OFFICE ACTION

In the Specification

The replacement specification paragraphs incorporate the following amendments. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

The paragraph beginning at line 22 on page 13 has been amended as follows:

Received from < 5098383424 > at 2/4/02 6:04:07 PM [Eastern Standard Time]

Another implementation is described with reference to Figs. 6-7. Like numerals from the first-described embodiment are utilized where appropriate, with differences being indicated with the suffix "b" or with different numerals. Fig. 6 is a sectional view or cut corresponding to that of Fig. 2, and depicts processing occurring subsequent to that of Fig. 2. Accordingly, an array 10b in accordance with this particular preferred embodiment is processed initially to the point as depicted in Fig. 2 in the first-described embodiment. A series of alternating trench isolation regions 22 and active areas 18 are thereby provided within semiconductor substrate 11 in a line adjacent and along at least a portion of lines of floating gates 12 and 14. Such defines a series of discrete transistor source areas separated by trench isolation regions. Floating gate word line patterning thereafter occurs, followed by drain region formation as described above. Lines of floating gates 12 and 14 as depicted in Fig. 7 (as well as in Figs. 8 and 9 described subsequently) comprise a gate dielectric layer, floating gate regions 23 formed thereover, an interpoly dielectric layer formed over floating gate regions 23, a conductively doped polysilicon/silicide stack formed over the interpoly dielectric layer, and an insulative cap formed over the conductively doped polysilicon/silicide stack.

Received from < 5098383424 > at 2/4/02 6:04:07 PM [Eastern Standard Time]

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

24. (Amended) A method of forming a line of FLASH memory cells comprising:

forming a line of floating gates over a semiconductor substrate;

providing an alternating series of trench isolation regions and active area regions in the semiconductor substrate in a line adjacent and along at least a portion of the line of floating gates, the series of active areas defining discrete transistor source areas separated by trench isolation regions, the trench isolation regions comprising isolation trenches having insulating dielectric material received therein;

forming a conductive line over the discrete transistor source areas and ~~trench isolation regions separating same~~ over the insulating dielectric material received within the isolation trenches adjacent and along at least a portion of the line of floating gates, the conductive line electrically interconnecting said discrete transistor source areas; and

providing source forming conductivity enhancing impurity into the discrete transistor source areas.

Received from < 5098383424 > at 2/4/02 6:04:07 PM [Eastern Standard Time]

36. (Amended) A method of forming a line of FLASH memory cells comprising:

forming a line of floating gates over a semiconductor substrate, the line of floating gates having a source side and a drain side, the line of floating gates having an insulative cap having an outermost surface;

depositing an insulative sidewall forming layer over the line of floating gates; and

in one anisotropic etching step of the insulative sidewall forming layer, forming an insulative sidewall spacer on only ~~one of the source side and~~ the drain side and not ~~the other~~ on the source side, the insulative sidewall spacer having an outermost surface which is substantially elevationally coincident with the insulative cap outermost surface.

Received from < 5098383424 > at 2/4/02 6:04:07 PM [Eastern Standard Time]

37. (Amended) [The m thod of claim 36] A method of forming a line of FLASH memory cells comprising:

forming a line of floating gates over a semiconductor substrate, the line of floating gates having a source side and a drain side, the line of floating gates having an insulative cap having an outermost surface;

depositing an insulative sidewall forming layer over the line of floating gates;

in one anisotropic etching step of the insulative sidewall forming layer, forming a first insulative sidewall spacer on only one of the source side and the drain side and not the other, the first insulative sidewall spacer having an outermost surface which is substantially elevationally coincident with the insulative cap outermost surface; and

further comprising in another anisotropic etching step, forming ~~an~~ a second insulative sidewall spacer on the other side, the second insulative sidewall spacer having an outermost surface which is substantially elevationally coincident with the insulative cap outermost surface.

40. (Amended) The method of claim ~~36~~ 37 wherein the one side is the source side.

Received from < 5098383424 > at 2/4/02 6:04:07 PM [Eastern Standard Time]

41. (Am nded) The method of claim ~~36~~ 37 wherein the one side is the drain side.

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